REMARKS

Applicants wishe to thank the Examiner for the attention accorded to the instant application.

Claims 1, 2, 5, 7, 11, 13, 14, 17, 19, 23, 25, 31, 35, 55, 60, 61, 68 and 72 are pending in the application. Applicants have amended claims 1, 55, 60, 61 and 72. Applicants have added new claim 74.

I. Claim Rejections – 35 U.S.C. § 102

The Examiner has rejected claim 72 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application Publication No. 20010022739 to Funaba et al. ("Funaba"). The Examiner asserts that Funaba discloses all of the essential limitations of claim 72.

Applicants respectfully traverse. Claim 72 has been amended to more particularly point out and distinctly claim the subject matter regarded as the invention. The present invention, in one aspect, is a semiconductor package having two surfaces with at least two ball terminal adhesive areas for each input/output signal coupled to memory chips. The chip pads formed by the two ball terminal adhesive areas make it possible for ease of suitable wiring layouts for either shortening the wire lengths or for uniform wiring lengths across the semiconductor package.

Funaba does not teach or suggest the use of ball terminal adhesive areas as required by claim 72. Funaba is directed to a memory system with modular data and power wirings where each individual modular data wiring is not constituted to be a branch of the system data wiring so that data signal reflections are minimized. The Examiner asserts that FIGs. 38A and 38B of Funaba teach the ball terminal adhesive areas as recited in claim 72. However, Applicants respectfully submit that FIGs. 38A and 38B do not show, *inter alia*, any ball terminals.

Furthermore, there is no mention in Funaba of any ball terminal or terminal adhesive for coupling to the input/output signals.

Since the cited reference does not disclose each and every limitation recited in the amended claims, Applicants respectfully submit that independent claim 72 is allowable over the cited reference. Early notice to that effect is earnestly solicited.

II. Claim Rejections – 35 U.S.C. § 103

The Examiner has rejected claims 1, 5, 55, 60-61 and 68 under 35 U.S.C. §103(a) as being unpatentable over Funaba in view of U.S. Patent No. 6,630,628 to Devnani et al. ("Devnani"). The Examiner has rejected claim 2 under 35 U.S.C. §103(a) as being unpatentable over Funaba in view of Devnani in further view of U.S. Patent No. 6,137,164 to Yew et al. ("Yew"). The Examiner has rejected claim 7 under 35 U.S.C. §103(a) as being unpatentable over Funaba in view of Devnani in further view of U.S. Patent No. 6,184,477 to Tanahashi ("Tanahashi").

Claims 1, 5, 55, 60-61 and 68:

The Examiner has rejected claims 1, 5, 55, 60-61 and 68 as being unpatentable over Funaba in view of Devnani. The Examiner asserts that Funaba discloses all of the essential limitations of claims 1, 5, 55, 60-61 and 68 except that Devnani teaches input/output pads on a chip being used to mount the chip on a substrate.

Applicants respectfully traverse. Claims 1, 55, 60 and 61 have been amended to more particularly point out and distinctly claim the subject matter regarded as the invention. The present invention, in one aspect, is a semiconductor unit with two device terminals for each input/output signal where the device terminals are connected to both ends of a signal wire. The

present invention recognizes that high speed operation of a memory system requires precise timing control over factors such as wire lengths and wire timing delays. By providing at least two terminals for each of the input/output signals, flexibility in wiring is introduced, especially for data lines in memory systems.

The Examiner's cited base reference, Funaba, is fundamentally different. Funaba does not teach or suggest the use of at least two terminals for each of the input/output signals. Funaba is directed to a memory system with modular data and power wirings where each individual modular data wiring is not constituted to be a branch of the system data wiring so that data signal reflections are minimized. The Examiner asserts that FIG. 50 of Funaba teaches the use of two terminals for each of the input/output signals. Applicants respectfully disagree. Data signal wiring 112 is clearly coupled only to one terminal in the profile view of the Funaba device. In fact, Funaba does not even recognize nor discuss the problem of wire flexibility – a problem solved by the present invention.

Devnani does not overcome the shortcomings of the Funaba reference. Devnani is directed to multi-layer laminated substrates for mounting semiconductor devices. However, Devnani does not teach or suggest the use of at least two device terminals for each input/output signal.

There is no prima facie case of obviousness. Even if the combination were proper, the proposed combination of Funaba and Devnani is not the same as the claimed invention. Applicants respectfully submit that one of ordinary skill in the art at the time the invention was made would have modified the teachings of Funaba with Devnani to produce a memory system supported by a multi-layer substrate with modular data and power wirings so that data signal reflections are minimized.

Therefore, Applicants respectfully submit that a combination of Funaba and Devnani does not teach or suggest every claimed feature of the invention. The prior art reference (or references) must teach or suggest all of the claim limitations. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991). Since a prima facie case of obviousness has not been set forth, Applicants respectfully submits that claims 1, 55, 60 and 61 are allowable over the cited references. Claims 5 and 68, which depend from claims 1 and 61 respectively, are similarly allowable.

Claim 2:

The Examiner has rejected claim 2 as being unpatentable over Funaba in view of Devnani and further in view of Yew. The Examiner asserts that Funaba and Devnani discloses all of the essential limitations of claim 2 except that Yew teaches a semiconductor chip with an input and output buffer, an input protection resistor, and an electrostatic protection element.

Applicants respectfully traverse. Claim 2 depends from claim 1. There is no prima facie case of obviousness based on the combination of Funaba and Devnani as discussed above for independent claim 1. Yew does not overcome the shortcomings of the proposed combination of Funaba and Devnani.

Yew is directed to an integrated circuit semiconductor package stacked on both surfaces of an interposed body. The combination of Funaba, Devnani and Yew still requires at least two device terminals for each input/output signal. Such use of at least two device terminals is not taught or suggested by the references, either combined or individually. Therefore, Applicants respectfully submit that a combination of Funaba, Devnani and Yew does not teach or suggest every claimed feature of the invention. The prior art reference (or references) must teach or suggest all of the claim limitations. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991). Since a prima

facie case of obviousness has not been set forth, Applicants respectfully submits that claim 1 is allowable over the cited references. Claim 2, which depend from claim 1, is similarly allowable.

Claim 7:

The Examiner has rejected claim 7 as being unpatentable over Funaba in view of Devnani and further in view of Tanahashi. The Examiner asserts that Funaba and Devnani discloses all of the essential limitations of claim 7 except that Tanahashi teaches a signal layer between a power layer and a ground layer.

Applicants respectfully traverse. Claim 7 depends from claim 1. There is no prima facie case of obviousness based on the combination of Funaba and Devnani as discussed above for independent claim 1. Tanahashi does not overcome the shortcomings of the proposed combination of Funaba and Devnani.

Tanahashi is directed to a multi-layer substrate with orthogonal grid ground and power planes in the substrate. The combination of Funaba, Devnani and Tanahashi still requires at least two device terminals for each input/output signal. Such use of at least two device terminals is not taught or suggested by the references, either combined or individually. Therefore, Applicants respectfully submit that a combination of Funaba, Devnani and Tanahashi does not teach or suggest every claimed feature of the invention. The prior art reference (or references) must teach or suggest all of the claim limitations. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991). Since a prima facie case of obviousness has not been set forth, Applicants respectfully submits that claim 1 is allowable over the cited references. Claim 7, which depend from claim 1, is similarly allowable.

III. Allowable Subject Matter

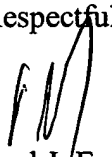
The Examiner has indicated that claims 11, 13, 14, 17, 19, 23, 25, 31 and 35 have allowable subject matter. The Examiner has objected to claim 11 as being dependent upon a rejected base claim, but indicated that the claim would be allowable if rewritten in independent form including all of the limitations of any intervening claims.

Applicants wish to thank the Examiner for the indication of allowable subject matter. By this amendment, Applicants are submitting new claim 74 which is claim 11 rewritten in independent form.

IV. Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections, and that they be withdrawn. The Examiner is invited to telephone the undersigned representative if an interview might expedite allowance of this application.

Respectfully submitted,



Paul J. Esatto, Jr.
Registration No. 30,749

Scully, Scott, Murphy & Presser, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343
PJE:dg